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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/517,471
Filing Date: December 07, 2004
Appellant(s): WAGNER ET AL.

William S. Francos
Reg. No. 38,456
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/28/08 appealing from the Office action mailed 2/7/08.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,307,480	Sheldon et al.	10-2001
7,051,332	Gatto et al.	5-2006

6,992,877 DeVries et al. 1-2006

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-6, 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Sheldon (United States Patent No 6,307,480). As per the claims, Sheldon discloses:

1. A method of monitoring the operation of at least one microcontroller unit associated with a system, the method comprising:

associating at least one monitoring module with the microcontroller unit has (column 3, lines 46-51),

resetting of the microcontroller unit (column 4, lines 30-44); and

acknowledging the resetting to the monitoring module by transmitting at least one confirming signal (column 4, lines 55-63), wherein the confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operations of the

microcontroller unit or is permitted only once by the monitoring module or both (column 4, lines 34-62).

3. A method as claimed in claim 1 wherein,

in relation to the operation of the microcontroller unit, a distinction is made between different reset events (column 4, lines 34-44:RS does not clear until Acknowledged) and in that

these different reset events are acknowledged to the monitoring module (10) by means of different confirming signals (ACK is only generated once per reset).

4. A base chip adapted to monitor operation of at least one microcontroller unit the base chip comprising:

at least one reset unit connected to the microcontroller and adapted to reset the microcontroller unit (column 4, lines 55-63), and at least one monitoring module that is associated with the microcontroller unit and to which the fact that a reset of the microcontroller unit had taken place can be acknowledges by at least one confirming signal (column 4, lines 46-51), wherein the confirming signal is formed by at least one trigger signal or trigger code that differs from the normal operation of the microcontroller unit or is permitted only once by the monitoring module or both (column 4, lines 34-44).

5. A base chip as claimed in claim 4, wherein

at least one information unit that is provided to allow for different reset events (column 4, lines 34-44), and

at least one supply unit that is connected to the microcontroller unit (it is inherent that a process requires power supply).

6. A base chip as claimed in claim 4 wherein

the monitoring module is adapted to be triggered f at least one interface unit or (column 3, lines 46-51).

to distinguish between individual accesses to the monitoring module different reset events can be marked by different trigger values or both.

8. A base chip as claimed in claim 4, wherein at least one signal line is provided between the monitoring module and the microcontroller unit, the signal line operative to transmit the confirming signal, the confirming signal including a trigger signal or a trigger code that differs from a normal operation of the microcontroller unit (column 4, lines 34-44).

9. A control system comprising at least one microcontroller unit (item 14) and at least one base chip (12) as claimed in claim 4.

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sheldon (United States Patent No 6,307,480).

As per claim 7, Sheldon does not explicitly disclose the use of a failsafe mode. Sheldon does disclose a special mode wherein the microprocessor goes into a constant reset mode if the reset is not acknowledged properly preventing the microprocessor from operating (column 4, lines 55-60).

Official Notice is given that it is notoriously well known to implement low power fail-safe modes in devices which are unable to properly reset. This is done so that the device unable to effect the system it is incorporated. In many system where power is at a premium, such satellites, small electronics and automobiles where power can come at a premium, reducing the power drain by a non-functional device is desirable and often practiced. thus it would have been obvious to modify Sheldon's safety feature of the continuous reset into a disabling to a low-power failsafe mode, thus allowing the

remainder of the system to operate with concern for error from the device and return the power to the system rather than powering a faulty device.

(10) Response to Argument

Applicant argues the limitation of "confirming signal is formed by at least one trigger signal **OR** trigger code that differs from the normal operations of the microcontroller unit **OR** is permitted only once by the monitoring module **OR** both" is not taught by Sheldon. While it not required by the claim due to Applicant use of "or" and as such simply having a trigger signal would suffice, Sheldon discloses every combination of limitations.

Sheldon discloses these items as described below:

1.) trigger signal that differs from the normal operations of the microcontroller unit (pulses the reset complete signal: column 4, line 56),

2.) or trigger code that differs from the normal operations of the microcontroller unit (pulses the reset complete signal: column 4, line 56. high indicates that it is digital signal with a value of "1" and is thus a code).

3.) is permitted only once by the monitoring module (column 4, lines 45-63: the RS logic gate is specifically designed only operate on the first trigger pulse. This is a fundamental property of RS latches (Reset-Set Latches).

4.) both. See above.

As such, the Examiner feels that all the limitations have been met with regards to the rejections under 35 USC §102. Resetting due to failure is not a normal operating condition, as it is in response to a failure.

Concerning the use of Official Notice, the Examiner notes Applicant has attempted to traverse rejection under MPEP 2144.03 C : *To adequately traverse such a finding, an applicant must specifically point out the supposed errors in the examiner's action, which would include stating why the noticed fact is not considered to be common knowledge or well-known in the art. See 37 CFR 1.111(b). See also Chevenard, 139 F.2d at 713, 60 USPQ at 241 ("[I]n the absence of any demand by appellant for the examiner to produce authority for his statement, we will not consider this contention."). A general allegation that the claims define a patentable invention without any reference to the examiner's assertion of official notice would be inadequate.*

In order to expedite this case before the board the Examiner has provided two pieces of supporting prior art.

Devries (6,992,877) discloses the use of counters to prevent multiple resets in the electronic demolitions environment.

Gatto (7,051,332) discloses the use of a counter/timer system to prevent multiple resets in an engine control system.

Both systems prevent multiple resets for safety and efficiency reasons, and are from widely disparate arts showing the basis for the stating that the concept of preventing multiple resets is widely help among engineers, and is used to solve multiple implementations.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Bryce P Bonzo/
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